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PATENT GROUP
CHOATE, HALL & STEWART
EXCHANGE PLACE, 53 STATE STREET
BOSTON, MA 02109

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/550,405	IO, EIJI
	Examiner	Art Unit
	ori nadav	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,9-11 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9-11 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The amendment to page 12, line 9, filed on 05/09/2005, is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention.

Applicant is required to cancel the new matter in the reply to this Office Action.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, additional diffusion layers formed below the lightly and heavily doped regions, as recited in claims 3 and 9, additional must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 3-7, 9-11 and 20-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification, as filed, for all of said at least one second heavily doped drain and source diffusion layer that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as

recited in claims 1 and 6, because said at least one second heavily doped drain and source diffusion laver is formed around said gate electrode, and said at least one second heavily doped drain and source diffusion layer that is located on the left side of the gate electrode does not have a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset.

There is no support in the specification for additional diffusion layers formed below the lightly and heavily doped regions, as recited in claims 3 and 9.

Claims 3-4 and 9-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of said at least lightly doped first and heavily doped second source and drain regions, as recited in claims 3-4 and 9-10, are unclear as to which elements are recited.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-4, 6, 9-10, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al.

Cheng et al. teach in figure 15 a semiconductor device comprising:

(a) a semiconductor substrate 11;

(b) an insulating film 19 formed at a surface of said semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated;

(c) a gate electrode 28 formed on said semiconductor substrate, said gate electrode and said insulating film defining at least one lightly doped first drain and source diffusion layer 77', 78';

(d) at least one sidewall 66 covering said gate electrode therewith; and

(e) at least one heavily doped second drain and source diffusion layer 82, 84 formed at a surface of said semiconductor substrate around said gate electrode,

said at least one sidewall having connected thereto a sidewall offset extending outwardly of said gate electrode along the surface of said semiconductor substrate in at least one of regions below which said at least one heavily doped second drain and source diffusion layer is to be formed, said sidewall offset having a lateral dimension extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a thickness of said sidewall,

(f) low resistive wiring layers 64 formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset,

said at least one heavily doped second drain and source diffusion laver extending below said sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said surface of said semiconductor substrate,

wherein all of said at least one second heavily doped drain and source diffusion laver that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with (parallel aligned with) the lateral dimension of said sidewall offset.

Cheng et al. do not teach in the embodiment of figure 15 at least one lightly doped first drain and source diffusion layers surrounding at least one heavily doped second drain and source diffusion layers on at least a bottom and a lateral side and extending towards the gate electrode beyond an edge of the sidewall offset.

Cheng et al. teach in the embodiment of figure 7 first drain and source diffusion layers 43, 44 surrounding second drain and source diffusion layers 57, 58 on at least a bottom and a lateral side, wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset, in Cheng et al.'s device, in order to improve the device characteristics by forming LDD regions in the device, and in order adjust and

optimize the device characteristics by extending the first drain and source diffusion layers towards the gate electrode beyond an edge of the sidewall offset.

Regarding claims 21 and 23, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

Claims 5, 7, 11, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Kunishima et al.

Cheng et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a silicide layer comprising titanium silicide.

Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice may be taken.

Regarding claims 5 and 11, Kunishima et al. teach using the semiconductor device as a CMOS device, and it is well known in the art that CMOS devices are used as memory devices. It would have been obvious to a person of ordinary skill in the art at the time

the invention was made to use Cheng et al.'s device as a memory device, because the intended use of a device depends on the requirements of the application in hand. Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 21 and 23, Kunishima et al. teach in figure 5C a sidewall entirely covering the gate electrode. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

Claims 20 and 22, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. in view of Gonzalez (5,439,835)

Cheng et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a sidewall offset extending in only one direction towards the source and drain diffusion layers.

Gonzalez teaches in figure 9 a sidewall offset extending in only one direction towards the source and drain diffusion layers.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a sidewall offset extending in only one direction towards the source and drain diffusion layers in Cheng et al.'s device, in order to improve the characteristics of the device.

Response to Arguments

Applicant argues that figure 3 provides support for the claimed limitations of all of said at least one second heavily doped drain and source diffusion layer that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as recited in claims 1 and 6.

The disclosure clearly states that the formation of sidewall offsets 54 ensure that the drain and source diffusion layers 65 and 66 extend beyond the peripheral edges of the sidewall offsets 54, and reach the sidewalls 53. "That is, distal ends of the drain and source diffusion layers 65 and 66 are located below either the sidewall 53 or the sidewall offset 54". There is no support for the claimed limitations of all of said at least one second heavily doped drain and source diffusion layer that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as recited in claims 1 and 6.

Furthermore, the claimed structure requires a process of making, wherein all said at least one second heavily doped drain and source diffusion layer are aligned with the

lateral dimension of said sidewall offset. However, no method is recited in the disclosure regarding the alignment of all said at least one second heavily doped drain and source diffusion layer with the lateral dimension of said sidewall offset.

Applicant argues that prior art does not teach that all of said at least one second drain and source diffusion laver that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as recited in claims 1 and 6.

Cheng et al. teach all of said at least one second heavily doped drain and source diffusion laver that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and have parallel alignment with the lateral dimension of said sidewall offset. Therefore, Cheng et al. teach all of said at least one second heavily doped drain and source diffusion laver that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as recited in claims 1 and 6.

Applicant argues that Cheng et al. do not teach that all of said at least one second drain and source diffusion laver that is disposed at said surface of said semiconductor substrate has a lateral dimension along the surface of said

semiconductor substrate that is approximately equal to and aligned with the lateral dimension of said sidewall offset, as recited in claims 1 and 6, because layers 82 and 84 in figure 15 are not aligned with sidewall 66, and layers 57 and 58 in figure 7 are not aligned with the lateral dimension of the sidewall offset.

The broad recitation of the claim does not require that all of said at least one second drain and source diffusion laver has a lateral dimension along the surface of said semiconductor substrate that is approximately aligned with the lateral dimension of said sidewall offset in the vertical direction. Alignment of two elements is a relative term, and can be considered to be in any direction.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
June 10, 2005

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800